**RTL Design & Synthesis**

**Bank Lock Vault Controller**

**Project Report**

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**INTRODUCTION**

The electronic lock is often introduced to illustrate the possibilities of design of an electronic system using a top-down approach. This is because it is not too complicated but must be designed as a complete system. The “customer” must be able to specify the key data sequence and the sequence must be easily modified when required. As designs become more complex, it becomes more efficient to move away from ad-hoc methods and use tools that allow the design to be carried out at a higher level of abstraction.

The design of electronics to control any automated system is generally referred to as CODE LOCK MACHANISM. An application of this is design of electronic safe. The front panel of the safe is kept as simple as possible for the user to understand. A code locking mechanism that transmits information between a key and a locking mechanism secured against interception misuse, but flexible with respect to original equipment, replacement parts, and emergency functions, is obtained if the key code is, in each case, cryptographically encoded through a hardware encoder.

When the locking mechanism is first operated, a control element inductively coupled to a locking mechanism read-write unit with a new key once and in a non-over writable manner, transmits an indent number to the object memory. Object-specific identity data are also stored in the control element. With the latter, a key number from a key register of the control element is combined with the key code to read the ladder together with a roll-in random code into the set of first still-neutral keys and into the object memory. Thus, a key is valid only if the object-specific identity data are considered in its key code. The lock used in the electronic safe is basically a combinational lock. A combinational lock is a lock that requires the entering of a specific sequence of symbols to dislodge and open.

The symbols are typically numerical, letters and other types of symbols may also be used to formulate a sequence. Depending on whether the lock is single-dial, multiple-dial; or discs or keypads may be used to enter sequences. Combinational locks are generally thought to be secure.

**AIM**

Create a Bank Valut Lock Controller using Verlog and implement it on Spartan 6 FGPA

**MAIN CODE**

**module Bank\_Valut\_Lock\_Controller(**

input clk, //system clock 100 MHz

input P, //President

input [1:0] VP,//VicePresidents

input Open, //Bank Open (1) or Closed (0)

output reg [15:1] LED, //starts blinking when unlock

output Unlock //stays solid, right most led on Basys 3 Board

);

//led assign to indicate whether the Vault is UNLOCK or not. Led ON means Vault Unlocked

assign Unlock = (P&VP[1]) | (P&VP[0]) | (Open&P) | (Open&VP[1]&VP[0]);

//slow clock 0.5s for blinking leds, when Vault is unlocked/open

wire slow\_clock;

clock\_half\_sec U0(clk,slow\_clock); ////slow clock 1s for blinking leds

//led blinking when Vault is unlock

always@ (posedge slow\_clock)begin //half a second

if ((P&VP[1]) | (P&VP[0]) | (Open&P) | (Open&VP[1]&VP[0])==1)

begin

LED<=~LED;

end

else

LED<=15'b0000000000000000;

end

endmodule

**module clock\_half\_sec(** //half a second clock

input clk, //basys 3 board clock, 100 MHz

output reg clock\_half //half a second clock , 2 Hz

);

reg [28:0] count=0;

always@(posedge clk)

begin

count<=count+1;

if (count==49\_999\_999) //50 M, 0 to 499,999,999

begin

count<=0;

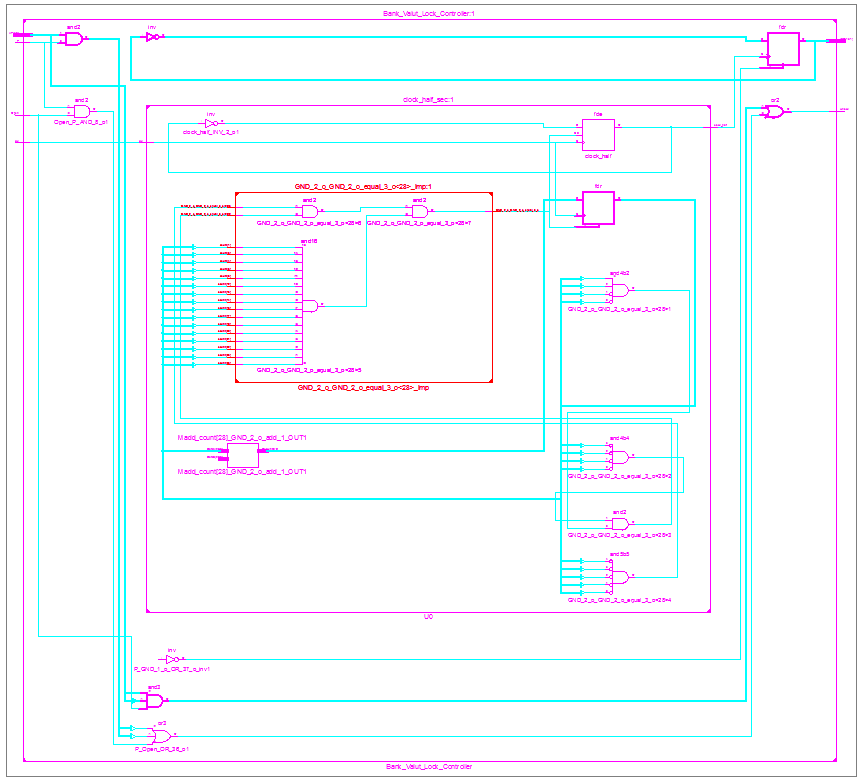
clock\_half=~clock\_half;

end

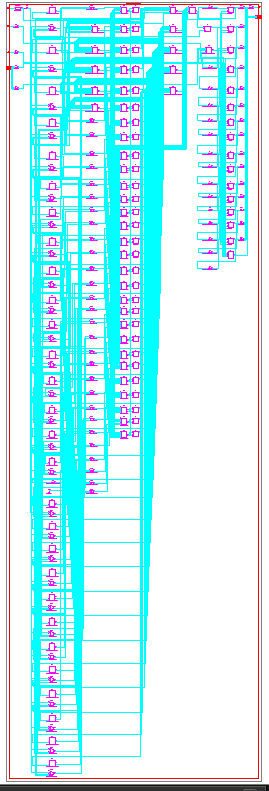
end

endmodule

**RTL SCHEMATIC**



**TECHNOLOGY SCHEMATIC**

****

**SOURCE CODE**

**# Clock signal**

NET "clk" LOC = "V10";

**#Switch to Open the Vault**

NET "Open" LOC = "T5";  
NET "P" LOC = "V8";  
NET "VP[0]" LOC = "U8";  
NET "VP[1]" LOC = "M8";

**#Leds**

NET "Unlock" LOC = "T11";  
NET "LED[1]" LOC = "R11";  
NET "LED[2]" LOC = "N11";  
NET "LED[3]" LOC = "M11";

**TEST BENCH**

module Bank\_tb;

// Inputs

reg clk;

reg P;

reg [1:0] VP;

reg Open;

// Outputs

wire [15:1] LED;

wire Unlock;

// Instantiate the Unit Under Test (UUT)

Bank\_Valut\_Lock\_Controller uut (

.clk(clk),

.P(P),

.VP(VP),

.Open(Open),

.LED(LED),

.Unlock(Unlock)

);

initial begin

// Initialize Inputs

clk = 1;

P = 0;

VP = 2'b00;

Open = 0;

// Wait 100 ns for global reset to finish

#100;

clk = 1;

P = 1;

VP = 2'b11;

Open = 0;

#100;

clk = 1;

P = 0;

VP = 2'b10;

Open = 0;

#100;

clk = 1;

P = 0;

VP = 2'b10;

Open = 1;

#100;

clk = 1;

P = 1;

VP = 2'b10;

Open = 0;

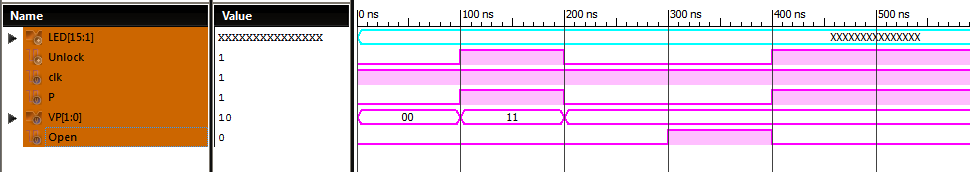
#100;

// Add stimulus here

end

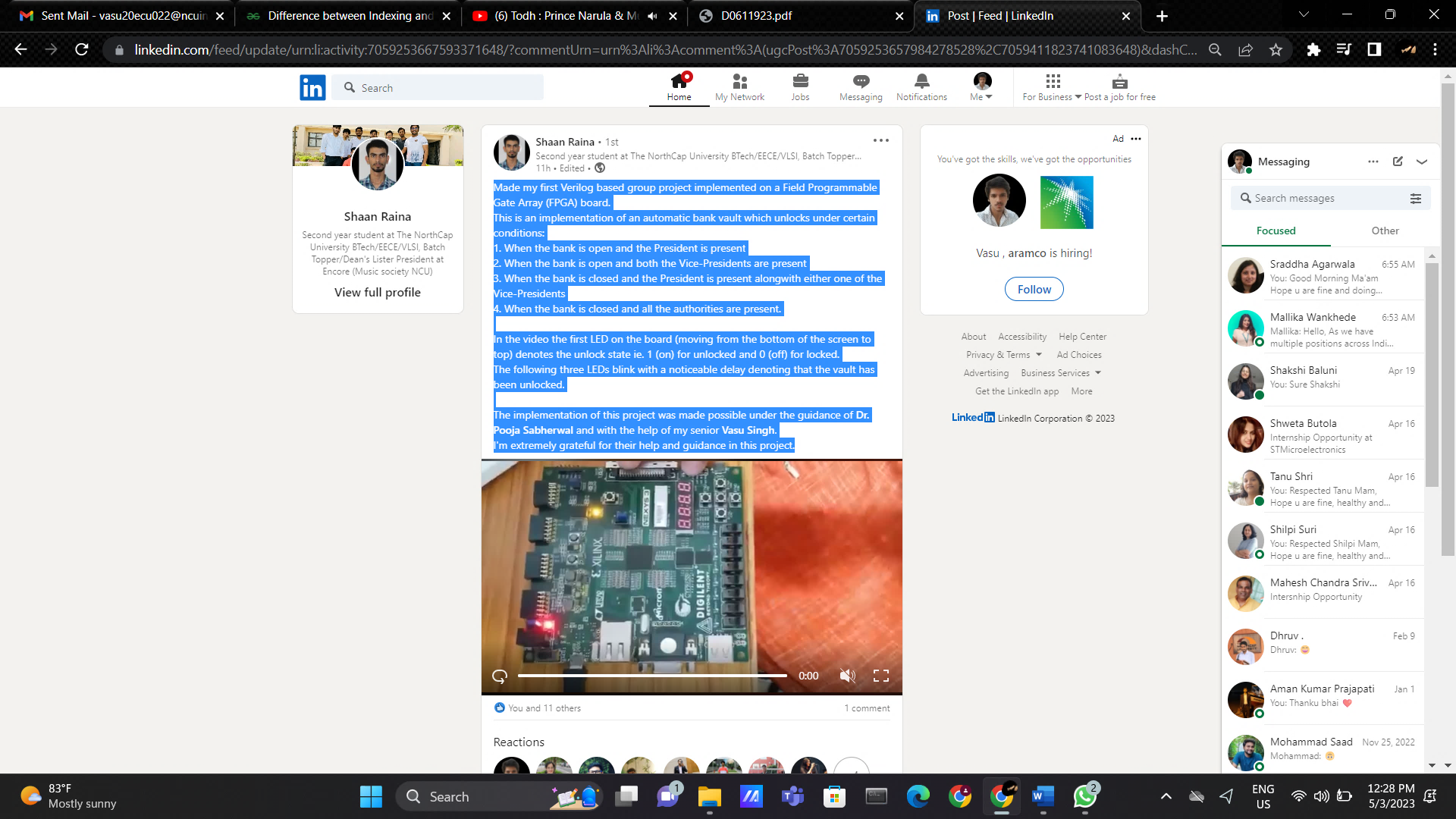
endmodule

**TIMING DIAGRAM**



**OUTPUT**

An automatic bank vault which unlocks under certain conditions:  
1. When the bank is open, and the President is present  
2. When the bank is open, and both the Vice-Presidents are present  
3. When the bank is closed, and the President is present along with either one of the Vice-Presidents  
4. When the bank is closed, and all the authorities are present.  
  
In the video the first LED on the board (moving from the bottom of the screen to top) denotes the unlock state i.e.. 1 (on) for unlocked and 0 (off) for locked.  
The following three LEDs blink with a noticeable delay denoting that the vault has been unlocked.



**CONCLUSION**

In the present scenario of the technology there are two fields in engineering that hold great demand in the industry, namely-communication & VLSI.

Therefore, in order to add glimpse to this development we thought of this research.A final point is that when a VHDL model is translated into the “gates and wires” that are mapped onto a programmable logic device such as CPLD or FPGA, then it is the actual hardware being configured, rather than the VHDL code being.When implementing the circuit in anti-fuse type FPGA, it is an advantage that the configuration file in memory is not necessary. In this case it is already verified that the circuit will be fully functional.